EAST Search History

Ref #	Hits	Search Query	DBs	Default Operator	Plurals	Time Stamp
L1	84	"6100594"	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 11:38
L2	2614151	controller microprocessor CPU processor	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 11:39
L3	254	stacked with memory with die	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 11:43
L4	193	3 and 2	US-PGPUB; USPAT; EPO; JPO; DERWENT; IBM_TDB	OR	ON	2006/10/27 11:43

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Application Number [ ] Submit

IDS Flag Clearance for Application 10809720

IDS Information

Content	Mailroom Date	Entry Number	IDS Review	Last Modified	Reviewer
M844	2006-08-09	33	Y ☑	2006-10-27 12:25:14.0	TNguyen31
M844	2004-03-25	13	Y ☑	2006-03-05 19:45:21.0	TNguyen31

Update

EAST - [thinhnew2.wsp:1]

File View Edit Tools Window Help

- S644: (369894) multilayer$2 multi adj layer$2
- S658: (327126) S635 S636 S637
- S659: (12) "6538331"
- S660: (2) "20050212144"
- S661: (0) die adj to adj die same connector
- S663: (949) die-to-die
- S662: (0) die adj to adj die
- S664: (2) S663 same connector
- S665: (236) S663 and memory and controller
- S667: (93) S663 and S666
- S666: (31982) wire near bond
- Favorites

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Default operator: OR

Plurals

Highlight all hit terms initially

S663 and S666

BRS form | ISR form | Image | Text | HTML

	U	1	Document ID	Issue Date	Pages	Title	Current OR	Current XRef	Retrieval Cla	Inventor	S	C	P	2	3	Image I
47			US 7023077 B2	20060404	23	Carrier with metal bumps for semiconductor die packages	257/678	257/679; 257/680;		Madrid; Ruben						US 7023
48			US 7018867 B2	20060328	7	Fabricating stacked chips using fluidic templated-assembly	438/110	257/723; 257/E21.705		Gracias; David						US 7018
49			US 7015587 B1	20060321	11	Stacked die package for semiconductor devices	257/777	257/666; 257/685;		Poddar; Anindya						US 7015
50			US 6998292 B2	20060214	11	Apparatus and method for inter-chip or chip-to-substrate connection with	438/107	257/685; 257/686;		McDonough; Robert J. et al.						US 6998
51			US 6979904 B2	20051227	8	Integrated circuit package having reduced interconnects	257/777	257/734; 257/780;		Farnworth; Warren M. et al.						US 6979
52			US 6965160 B2	20051115	17	Semiconductor dice packages employing at least one redistribution l	257/686	257/685; 257/698;		Cobbley; Chad A. et al.						US 6965
53			US 6956294 B2	20051018	17	Apparatus for routing die interconnections using intermediate c	257/786	257/E23.02; 257/E23.021;		Ball; Michael B.						US 6956
54			US 6949410 B2	20050927	16	Flip chip in leaded molded package and method of manufacture thereof	438/111	138/112; 138/116;		Joshi; Rajeev et al.						US 6949
55			US 6933223 B1	20050823	12	Ultra-low loop wire bonding	438/617			Soon; Lim Peng et al.						US 6933
56			US 6906408 B2	20050614	16	Assemblies and packages including die-to-die connections	257/686	257/724; 257/777;		Cloud; Eugene H. et al.						US 6906
57			US 6897096 B2	20050524	17	Method of packaging semiconductor dice employing at least one redistribut	438/123	257/E21.502; 257/E21.512;		Cobbley; Chad A. et al.						US 6897
58			US 6893901 B2	20050517	22	Carrier with metal bumps for semiconductor die packages	438/122	257/E23.069; 438/666;		Madrid; Ruben						US 6893
59			US 6787901 B2	20040907	12	Stacked dies utilizing cross connection bonding wire	257/724	257/735; 257/776;		Reyes; Edward et al.						US 6787
60			US 6720642 B1	20040413	17	Flip chip in leaded molded package and method of manufacture thereof	257/673	257/502; 257/578;		Joshi; Rajeev et al.						US 6720
61			US 6680219 B2	20040120	11	Method and apparatus for die stacking	438/109	228/180.5; 257/E25.011;		Reyes; Edward et al.						US 6680
62			US 6630372 B2	20031007	17	Method for routing die interconnections using intermediate c	438/123	257/E23.02; 257/E23.021;		Ball; Michael B.						US 6630
63			US 6603072 B1	20030805	8	Making leadframe semiconductor	174/536	257/686;		Foster; Donald C. et al.						US 6603

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